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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nguyen et al.	Attorney Docket No.: NSC1P131X1
Application No.: 10/080,913	Examiner: Farahani, Dana
Filed: February 21, 2002	Group: 2891
Title: METHOD AND APPARATUS FOR FORMING AN UNDERFILL ADHESIVE LAYER	Confirmation No. 1176

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on December 23, 2005 in an envelope addressed to the Commissioner for Patents, Mail Stop Appeal Brief-Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

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Agnes Spence

APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

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Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on November 14, 2005.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for months has already been secured and the fee paid therefor of $ is deducted from the total fee due for the total months of extension now requested.

☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an

extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.

Total Fee Due:

Appeal Brief fee	$500.00
Extension Fee (if any)	$
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☒ Enclosed is Check No. 28872 in the amount of $500.00.

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 500388, (Order No. NSC1P131X1).

Respectfully submitted,
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE NGUYEN, LUU et al.

Application for Patent

Filed February 21, 2002

Serial No. 10/080,913

FOR:

METHOD AND APPARATUS FOR FORMING AN UNDERFILL ADHESIVE LAYER

APPEAL BRIEF

BEYER WEAVER & THOMAS, LLP
Attorneys for Applicants

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Signed: _____
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(h) Claims 40-42 are patentable over the combination of Nishiguchi in view of Holzapfel.

I. REAL PARTY IN INTEREST

The real parties in interest is the assignee, National Semiconductor Corporation, Santa Clara, CA.

II. RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences related to this application.

III. STATUS OF THE CLAIMS

The current status of the claims is as follows:

(a) claims 1-18 have been cancelled; and

(b) claims 19-43 are pending and are the subject of this Appeal.

IV. STATUS OF THE AMENDMENTS AFTER FINAL

The Examiner issued a Final Rejection in the present application on October 19, 2005. After reviewing the file, the attorney for the applicants realized that claims 38-43 were inadvertently made dependent on claim 34. Claims 38-43 should have been dependent on independent claim 35. In a telephone interview with the Examiner, the Examiner agreed to change the dependency of claim 38-43 from claim 34 to claim 35. Pursuant to the verbal agreement, the applicants submitted an Amendment H on November 17, 2005, changing the dependency of the claims. In an Advisory Action dated December 5, 2005, the Examiner refused to enter the amendment. Claims 38-43 remain dependent on claim 34.

V. SUMMARY OF THE INVENTION

The present invention relates to an improvement for a certain type of semiconductor package often referred to as a "flip chip". A typical flip chip 102 is illustrated in Fig. 1(b) of the present application. The flip chip 102 includes solder balls 106 formed on the active surface (i.e., the top surface of the chip) as illustrated in the figure provided below.

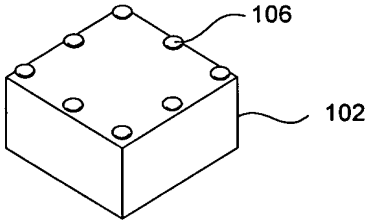


Fig. 1(b)

The device 102 is called a flip chip because it is flipped up-side-down and mounted onto a substrate such as a printed circuit board or substrate. The solder bumps 106 are then reflowed to electrically connect the die to the substrate. When a flip chip 102 is mounted to the substrate, an air gap typically remains between the device and substrate. In the prior art, this gap is commonly filled with a liquid underfill material that is flowed into the gap by capillary action and is then solidified. There are several problems associated with this type of underfill process. Namely, the underfill material must be applied individually to each flip chip mounted onto a substrate. Also, the underfill material may not evenly flow within the gap, resulting in uneven edges of the underfill material at the interface of the flip chip and substrate around the periphery of the device.

To avoid the aforementioned problems, the present invention is directed to applying a layer of underfill adhesive on the flip chips 102 while still in wafer form. With the present invention, a plurality of the flip chips, separated by the scribe lines 104, are first fabricated on the active surface of a wafer 100 (see Figure 1(a)).

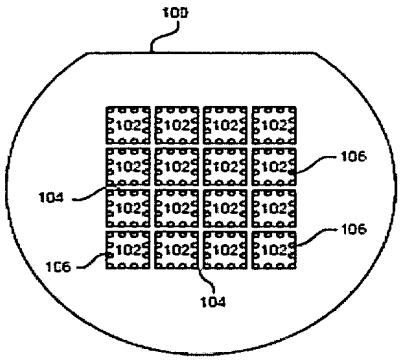


Fig. 1(a)

After circuit fabrication, the solder balls 106 are formed on the individual chips 102 on the wafer. A re-flowable underfill material 130 is next applied across the active surface of the wafer 100. Figures 3(a) and 3(b) illustrate partial cross sections of the wafer 100 after the underfill material 130 has been applied. In Figure 3(a), the underfill layer 130 is shown at a pre-cure height. After the underfill material is at least partially cured, the height is reduced exposing the solder balls 106, as illustrated in Figure 3(b). In various embodiments, the undefill material can be either partially or fully cured after being applied to the wafer.

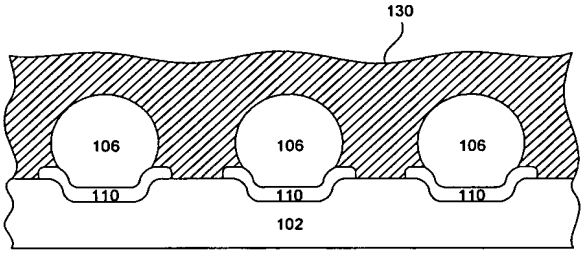


Fig. 3(a)

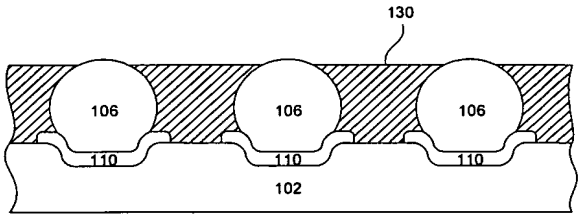


Fig. 3(b)

After the underfill material 130 is cured (either partially or fully), the individual chips are singulated by cutting the wafer along the scribe lines 104. Since the wafer is cut along the scribe lines, the underfill layer 130 on each individual chip has cut edges around the periphery. When the individual chip is mounted, it is flipped and placed downward with the solder balls in contact with the contacts on the substrate. The solder balls are then reflowed, causing them to form electro-mechanical bonds with the contacts on the substrate. During the solder reflow process, the underfill material 130 also reflows. As a result, filets 132 are formed around the periphery of the chip 102 and the substrate 120 as illustrated in Figure 4.

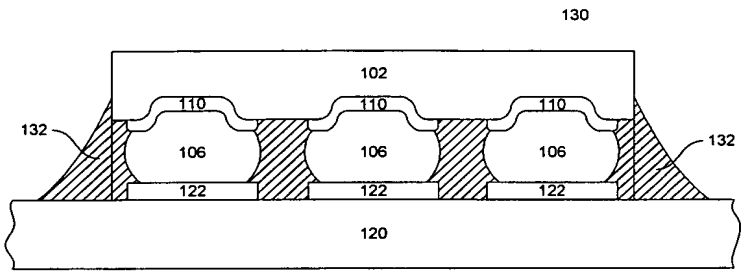


Fig. 4

The present invention provides a number of advantages over the prior art. Since the underfill material 130 is applied on the wafer level, there is no need to individually apply it in liquid form after each flip chip has been mounted onto the substrate. Secondly, the uniformity of the layer of underfill material 130 applied to the wafer results in a more even, uniform, bond between the flip chip and substrate than otherwise possible using the prior art method of relying on capillary action to introduce the liquid underfill material between the flip chip and substrate.

Claims 19-34 and 38-43 are directed to an individual flip chip after being fabricated in accordance with the procedure described above. The flip chip has solder balls and a layer of underfill adhesive formed on the active surface of the chip. Since the adhesive layer is applied onto the flip chip while still in wafer form, the adhesive has cut edges around the periphery of the chip after singulation.

Claims 35-37 are directed to a wafer having a plurality of flip chip die and solder balls formed thereon. A layer of at least partially cured underfill adhesive is formed on the active surface of the wafer.

VI. GROUNDS OF REJECTION TO BE REVIEWED

(a) Whether claims 19, 22-24 and 26-31 are patentable over the combination of Nishiguchi (US Patent 5,214,308) and Abe (US Patent 6,288,444)?

(b) Whether claims 20 and 25 are patentable over the combination of Nishiguchi, Abe and Kato (US Patent 6,486,562)?

(c) Whether claim 21 is patentable over the combination of Nishiguchi, Abe and Morihara (US Patent 5,495,439)?

(d) Whether claims 32-34 and 43 are patentable over the combination of Nishiguchi, Abe and Chiu (US Patent No. 6,391,683)?

(e) Whether claims 35, 36 and 39 are patentable over the combination of Nishiguchi in view of Holzapfel (US Patent 5,872,633)?

(f) Whether claim 37 is patentable over the combination of Nishiguchi in view of Holzapfel?

(g) Whether claim 38 is patentable over the combination of Nishiguchi in view of Holzapfel and Kato?

(h) Whether claims 40-42 are patentable over the combination of Nishiguchi in view of Holzapfel?

VIII. ARGUMENTS

(a) **Claims 19, 22-24 and 26-31 are patentable over the combination of Nishiguchi (US Patent 5,214,308) and Abe (US Patent 6,288,444)**

The Nishiguchi Reference

The Examiner is relying on Figures 2 and 3 of Nishiguchi in formulating the rejection. These figures are recreated below for convenience.

Fig. 2

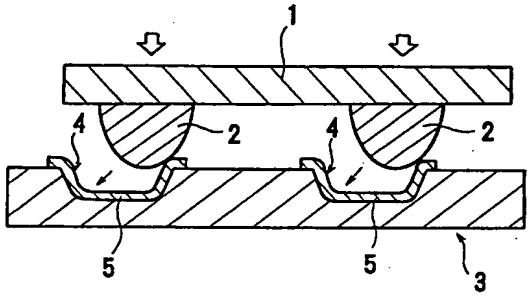
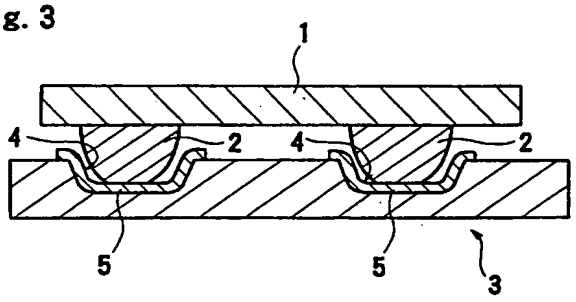


Fig. 3



The Nishiguchi reference teaches the filling of the gap between a semiconductor device 1 and a substrate 3 with a bonding agent ***after*** the semiconductor device has been mounted onto the substrate. Specifically, column 3 lines 46-52 state:

> Instead of molting the bump 2, insulative bonding agent which contracts when it cures may be **filled into a gap between the semiconductor device 1 and the substrate 3** and the bump 2 may be pushed to the electrode terminal 5 by a curing contraction force of the bonding agent to electrically connect the bump 2 to the electrode terminal 5. (emphasis added)

The bonding agent at the edges of the Nishiguchi reference are therefore not: (i) cut; or (ii) applied directly to the active surface of the semiconductor device while in wafer form.

The Abe Reference

The Abe reference is directed toward a fine pitch Ball Grid Array (BGA) package 10A for a semiconductor chip that generates a large amount of heat during operation. The package, as best illustrated in Figure 2 (provided below for convenience), includes a semiconductor chip 11 mounted within a rectangular opening located at the center of a printed wiring board 12A. See Column 4, lines 3-7. The chip 11 is in contact with a stage portion 24A of a metal heat spreader 13A. Solder balls 15, provided on the wiring board 12A, are used to mount the package onto a substrate. See column 3, lines 63-66. Wire bonds 19 are provided between the chip 11 and a wiring layer 16 of the printed wiring board 12A. See column 3, line 67 through column 4, line 2. A sealing resin 14A, including first and second sealing resin portions 26A and 27A, is provided on the package. The first resin portion 26A surrounds the chip 11. The second resin portion is formed on top of the stage portion 24A of the metal heat spreader 13A and extends to the outer periphery of the BGA package. See column 5, lines 14-22 and 65-68 and column 6, lines 1-6.

FIG. 2

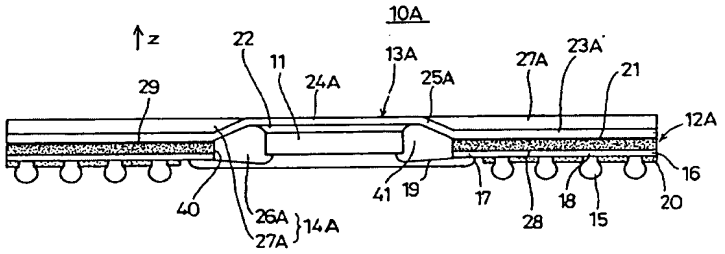
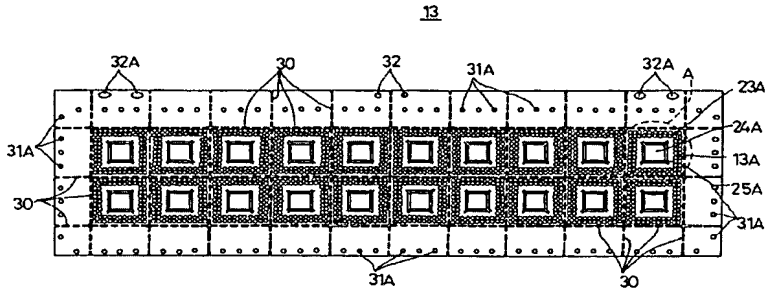


Figure 4 (provided below) of Abe shows a multi-cavity mold. During fabrication of the devices 10A, individual chips 11 and heat spreaders 13A are placed in a cavity. During a transfer molding process, the sealing resin including the two portions 26A and 27A are formed. See column 9, lines 58-67.

FIG. 4



Once the resin is transferred into the mold and hardened, the wiring board 12A is removed from the mold. The individual BGA packages are then marked, the solder balls 15 are formed, and then the wiring board is cut along the cutting slits 30. As clearly evident in the figure, the cutting slits 30 run along the horizontal and vertical directions, defining the boundaries between the individual BGA packages 10A in the multi-cavity mold.

The Rejection

Since Nishiguchi fails to teach a flip chip with a layer of underfill adhesive with cut edges, the Examiner has turned to the Abe reference. In formulating the rejection, the Examiner states that "***Abe discloses an underfill, 14 of figure 2 has cut edges at the periphery of the chip ...***" . A careful review of Abe, however, indicates that the Examiner has misconstrued the actual teaching of the reference. Figure 3 of Abe illustrates a flow chart for making the package illustrated in Figure 2. The final step, labeled "Cutting Step" or "S9" in Figure 3, is described in Column 10, lines 41-46 of Abe. After the package is fabricated as described above, it is cut along the "***outer periphery***" (emphasis added) of the packaged device 10A through the heat spreader 13, the printed wiring board 12A and the portion 27A of the sealing resin 14A. As noted above, the cutting is performed along the horizontal and vertical slits 30. The cutting step of Abe therefore does **not** teach the cutting of the portion 26A of the resin layer 14A around the periphery of the chip 11 as stated by the Examiner.

The Examiner has failed to demonstrate a prima facie case of obviousness of claim 19 for a number of reasons.

(i) **The References are Not Combinable**: Nishiguchi is directed to the filling of the gap between a semiconductor device and a substrate with a bonding agent after the semiconductor device has been mounted onto the substrate. Abe is directed to attaching a heat spreader using a resin to a plurality of BGA packages in a mold. The two references

are directed to two entirely different types of semiconductor packages and have absolutely nothing in common with each other. There is no teaching or suggestion in either reference whatsoever that would motivate one skilled in the art to combine the two as suggested by the Examiner.

(ii) **Even if the Proposed Combination was Proper, it Still Would not Result in the Present Invention as Claimed:** Claim 19 recites that: (i) the underfill adhesive has edges that are cut around the periphery of the flip chip; and (ii) the underfill material is applied directly to the active surface of the flip chip integrated circuit. Since the underfill material is applied to the flip chip of the present invention while in wafer form and then cut during the dicing operation, the edges of the die have clean "***cut***" straight vertical surfaces.

In contrast, the underfill material at the edges of the Nishiguchi device in comparison are likely to have uneven, non-straight, surfaces since the material is dispensed between the chip and the printed circuit board and then allowed to randomly flow before solidifying. Furthermore, the filling of the gap between the device and substrate of Nishiguchi is not the same as applying underfill adhesive directly to active surface of a flip chip.

A number of important distinctions exist between the present invention as claimed and the package described by Abe:

(i) the present invention is directed to a "***flip chip***" type integrated circuit package. The Abe reference is directed toward a BGA type package;

(ii) "***solder balls***" are formed on the "***active surface***" of the on the flip chip of the present invention. In contrast, there are no solder balls formed on the chip 11 of Abe. Rather, solder balls 15 are provided on the printed wiring board 12A;

(iii) the present invention defines a layer of "***underfill adhesive***" applied on the "***active surface***" of the flip chip. With the Abe reference, there is no underfill adhesive applied to the chip 11. The resin layer 14A is

for sealing the package, not an adhesive layer for mounting the Abe package to a substrate; and

(iv) the present invention defines the underfill as having "***cut edges***" around the periphery of the flip chip. In contrast, the cutting as taught by Abe occurs at the outer periphery of the printed wire board 12A (i.e., the outer periphery of the BGA package), not along the peripheral sides of the chip 11.

Thus, even if it were proper to combine the references, it still would not result in the present invention as claimed. Neither reference teaches, either alone or in combination, the present invention, (i.e., a flip chip having underfill adhesive formed thereon and with edges that are cut around the periphery of the flip chip). Nishiguchi teaches the introduction of an underfill material between the chip and a substrate after mounting, resulting in the underfill having uneven edges. Abe on the other hand teaches the application of a sealing resin 26A on a chip in a BGA package. The resin 26A, however, is never cut. Abe therefore also fails to teach a flip chip having an adhesive layer with cut edges around the periphery of the chip.

Claim 19 is therefore patentable over the Nishuguchi and Abe references.

Claim 22 covers the application of the underfill adhesive onto the active surface of the flip chip at a pre-cure height. Nishuguchi teaches the application of an underfil material after the chip has been mounted onto a substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 23 covers the pre-cure height of the underfill material ranging from 140% to 90% of the height of the solder balls. Nishuguchi teaches the application of an underfill material after the chip has been mounted onto a substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 24 covers the application of the underfill on the flip chip while still in wafer form. Nishuguchi teaches just the opposite, the application of an underfil material after the chip has been mounted onto a substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 26 covers a flip chip with an underfill adhesive layer having cut edges and solder balls formed on contact pads. Nishuguchi teaches the application of an underfil1

material after the chip has been mounted onto a substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 27 covers the underfill adhesive applied to the active surface of the flip chip as being either partially or fully cured. Nishuguchi teaches the application of an underfill material after the chip has been mounted onto a substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 28 covers the underfill adhesive being as being substantially opaque. Nishuguchi teaches the application of an underfill material after the chip has been mounted onto a substrate. Nishuguchi fails to teach or suggest anything regarding if the underfill material is opaque. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 29 covers the range of the coefficient of thermal expansion of the underfill material. Nishuguchi fails to teach or suggest any teaching regarding the coefficient Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 30 defines the melting point of the underfill adhesive. Nishuguchi fails to teach or suggest a melting point of the bonding agent used to mount the flip chip to the substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

Claim 31 covers the range of the elastic modulous of the underfill adhesive. Nishuguchi fails to teach or suggest an elastic modulous of the bonding agent used to mount the flip chip to the substrate. Abe fail to teach or suggest anything to do with using an underfill material. The claim is therefore patentable.

(b) Whether claims 20 and 25 are patentable over the combination of Nishiguchi, Abe and Kato (US Patent 6,486,562) ?

Kato is directed to a semiconductor package having a flip chip mounted into a BGA type package. As illustrated in Figure 3, the BGA package includes a flip chip 2 having solder balls 7 mounted onto a an interposer substrate 3. A heat sink 11 is provided on the top of the package, in contact with the back surface of the flip chip 2.

Solder balls 6 are provided along the bottom surface of the substrate 3. The space between the flip chip 2 and the substrate 3 is filled with a mold resin 101. The mold resin is formed using a transfer mold of an epoxy resin material. See column 7, lines 7-14.

Claim 20 further defines the undefill material applied to the active surface of the flip chip as being composed of a resin, hardener, catalyst, dye, and filler. Both Nishiguch and Kato discuss the application of some type of material between a flip chip and a substrate ***after*** it has been mounted. Since neither reference discloses a flip chip having an underfill adhesive with cut edges around the periphery, claim 20 is allowable.

As per claim 25, Kato teaches that a resin can be injection molded between a flip chip and a substrate. Since neither Kato or Nishiguchi disclose an underfill adhesive using epoxy, poly-imides, or silicon-polyimide copolymers, the claim is allowable.

(c) Whether claim 21 is patentable over the combination of Nishiguchi, Abe and Morihara (US Patent 5,495,439) ?

Claim 21 further defines the underfill adhesive as having a coefficient of thermal expansion similar to the substrate it is to be mounted on. Morihara is directed to a Silicon on Insulator (SOI) dynamic access memory (DRAM) chip. Morihara has absolutely nothing to do with flip chips or the formation of an underfill adhesive layer on the active surface of the flip chip. Claim 21 is therefore patentable.

(d) Whether claims 32-34 and 43 are patentable over the combination of Nishiguchi, Abe and Chiu (US Patent No. 6,391,683) ?

Chiu is directed to a flip chip wherein a metal dam is provided around the chip attach area of the substrate. The primary purpose of the dam 110a as illustrated in Figures 3A-3D and Figure 4 is to control the flow (i.e., the width) of the undefill material when it is applied between the flip chip and substrate using capillary action. See column 3, line 66 through column 4, line 14. The dam 110a of Chui is therefore formed

on the substrate the flip chip is to be mounted on, not the wafer the flip chips are fabricated on.

Claims 32 and 43 are directed to providing a dam around the periphery of the wafer, not the substrate upon which a flip chip is to be mounted. Claims 32 and 43 are therefore allowable.

Claims 33 and 34 are directed to the application of a solder paste and fluxing material onto the substrate the flip chip is to be mounted. Chui is directed to forming a dam around the die attach area of the substrate. Claims 33 and 34 are therefore patentable.

(e) Whether claims 35, 36 and 39 are patentable over the combination of Nishiguchi in view of Holzapfel (US Patent 5,872,633)

Claim 35 is directed to a semiconductor wafer with a layer of at least partially cured underfill adhesive formed on the active surface. As previously noted, Nishiguchi teaches the filling of the gap between an individual flip chip and a substrate with a bonding agent. Nishiguchi therefore explicitly teaches that the bonding agent is applied subsequent the semiconductor device being singulated from a wafer and is mounted onto the substrate. There is absolutely no mention in Nishiguchi that the bonding agent or a similar underfill material being applied to the flip chip while still in wafer form.

Holzapfel is directed to a polishing machine for removing layers from a wafer.

There is absolutely no reason whatsoever to combine Nishiguchi and Holzapfel. In fact, the two references seem to contradict one another, and therefore can not be combined as the Examiner suggests. One is directed to forming a layer (bonding agent) between a single semiconductor device and a substrate. The other is directed to removing layers from the surface of a semiconductor wafer.

Furthermore, even if it was proper to combine the two references, the proposed combination still would not teach the present invention. Neither reference teaches or suggests the application of an at least partially cured adhesive layer formed on the active surface of a flip chip semiconductor wafer.

The Applicants submit that claim 35 is therefore allowable.

Claim 36 is directed to applying the underfill adhesive to a pre-cure height. Since neither Nishiguchi or Holzapfel teach or suggest the application of an adhesive onto a flip chip wafer, claim 36 is allowable.

Claim 39 is directed to applying an opaque underfill adhesive onto a flip chip wafer. Since neither Nishiguchi or Holzapfel teach or suggest the application of an adhesive onto a flip chip wafer, claim 39 is allowable.

(f) Whether claim 37 is patentable over the combination of Nishiguchi in view of Holzapfel?

Claim 37 is directed to the pre-cure height of the underfill material on the wafer. In contrast, Nishiguchi is directed to applying the underfill material between a chip and a substrate after mounting the chip onto the substrate. Holzapfal is directed to the removal of layers on a semiconductor wafer. Claim, 37 is therefore patentable.

(g) Whether claim 38 is patentable over the combination of Nishiguchi in view of Holzapfel and Kato?

Nishiguchi is directed to applying the underfill material between a chip and a substrate after mounting the chip onto the substrate. Holzapfal is directed to the removal of layers on a semiconductor wafer. Claim, 37 is therefore patentable. Kato is directed to a semiconductor package having a flip chip mounted into a BGA type package. As illustrated in Figure 3, the BGA package includes a flip chip 2 having solder balls 7 mounted onto an interposer substrate 3. A heat sink 11 is provided on the top of the package, in contact with the back surface of the flip chip 2. Solder balls 6 are provided along the bottom surface of the substrate 3. The space between the flip chip 2 and the substrate 3 is filled with a mold resin 101. The mold resin is formed using a transfer mold of an epoxy resin material. See column 7, lines 7-14. None of these references, either alone or in combination, teach the invention of claim 38, which is the application of various types of epoxies and poly-imides onto the surface of a flip chip.

(h) Whether claims 40-42 are patentable over the combination of Nishiguchi in view of Holzapfel?

Nishiguchi is directed to applying the underfill material between a chip and a substrate after mounting the chip onto the substrate. Holzapfal is directed to the removal of layers on a semiconductor wafer. In contrast, claim 40 is directed to the coefficient of thermal expansion of the underfill adhesive. Claim 41 is directed to the melting range of the adhesive. Claim 42 is directed toward the elastic modulous of the adhesive. Since none of the these specifics are taught by the two references, either alone or in combination, claims 40-42 are allowable.

IX. CONCLUSION

In view of the foregoing, it is respectively submitted that all of the claims are patentably distinct over the art of record. Accordingly the pending rejections of all the pending claims should be reversed.

Respectfully Submitted,
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X. APPENDIX

1. - 18. (cancelled)

19. (previously presented) An apparatus, comprising:

a flip chip integrated circuit having flip chip bond pads with solder bumps formed directly an active surface of the flip chip; and

a substantially uniform layer of underfill adhesive applied directly on the active surface of the flip chip integrated circuit and around the solder bumps formed onto the active surface, the substantially uniform layer of underfill adhesive having cut edges around the periphery of the flip chip.

20. (original) The apparatus of claim 19, wherein the underfill adhesive includes one or more of the following components: an epoxy resin, a hardener, a catalyst initiator, a coloring dye, and an inorganic filler.

21. (previously presented) The apparatus of claim 19, wherein the underfill adhesive has a coefficient of thermal expansion substantially similar to that of the substrate upon which the flip chip integrated circuit is intended to be mounted.

22. (original) The apparatus of claim 19, wherein the underfill adhesive is deposited on the active surface of the flip chip integrated circuit at a pre-cured height such that the solder bumps are at least exposed through the underfill adhesive after curing.

23. (original) The apparatus of claim 22, wherein the pre-cured height of the underfill adhesive applied to the wafer ranges from 140% to 90% of the height of the solder bumps.

24. (previously presented) The apparatus of claim 19, wherein the underfill adhesive layer is deposited on the active surface of the flip chip integrated circuit in wafer form before the flip chip integrated circuit is singulated from the wafer.

25. (previously presented) The apparatus of claim 19, wherein the underfill adhesive is selected from the group comprising: epoxies, poly-imides, silicone-polyimide copolymers.

26. (previously presented) The apparatus of claim 19, wherein the substrate has a plurality of contact pads, the contact pads configured to contact the solder bumps of the flip chip when the flip chip is mounted onto the substrate, the contact pads and the solder bumps forming joints electrically connecting the flip chip to the substrate.

27. (previously amended) The apparatus of claim 19, wherein the underfill adhesive material is in one of the following states, either fully cured or partially cured.

28. (previously presented) The apparatus of claim 19, wherein the layer of underfill adhesive is substantially opaque thereby protecting the flip chip integrated circuit from photo induced leakage currents by blocking visible light.

29. (original) The apparatus of claim 19, wherein the underfill adhesive has a coefficient of thermal expansion in the range of approximately 20 x 10^{-6}/K to approximately 30 x 10^{-6}/K @ 25 ^{0}C.

30. (original) The apparatus of claim 19, wherein the underfill adhesive melts at between 120 to 140 degrees C and reacts at between 175 to 195 degrees C.

31. (original) The apparatus of claim 19, wherein the underfill adhesive has an elastic modulous in the range of 1 to 10 GPa.

32. (previously presented) The apparatus of claim 24, further comprising a dam around the periphery of the wafer to prevent the underfill material deposited onto the surface of the wafer from flowing off the wafer before the partial curing of the adhesive layer.

33. (previously presented) The apparatus of claim 26, wherein a solder paste is provided on the contact pads of the substrate.

34. (previously presented) The apparatus of claim 26, wherein a fluxing material is provided on the substrate.

35. (previously presented) An apparatus, comprising:

a semiconductor wafer having an active surface including a plurality of die formed thereon;

one or more bond pads formed on the plurality of die;

one or more solder bumps formed on the one or more bond pads respectively; and

a layer of at least partially cured underfill adhesive formed around the solder bumps on the active surface of the wafer.

36. (previously presented) The apparatus of claim 35, wherein the underfill adhesive is deposited on the active surface of the wafer at a pre-cured height such that the solder bumps are at least exposed through the underfill adhesive after the partial curing.

37. (previously presented) The apparatus of claim 35, wherein the pre-cured height of the underfill adhesive applied to the wafer ranges from 140% to 90% of the height of the solder bumps.

38. (previously presented) The apparatus of claim 34, wherein the underfill adhesive is selected from the group comprising: epoxies, poly-imides, silicone-polyimide copolymers.

39. (previously presented) The apparatus of claim 34, wherein the layer of underfill adhesive is substantially opaque.

40. (previously presented) The apparatus of claim 34, wherein the underfill adhesive has a coefficient of thermal expansion in the range of approximately 20 x 10^{-6}/K to approximately 30 x 10^{-6}/K @ 25 ^{0}C.

41. (previously presented) The apparatus of claim 34, wherein the underfill adhesive melts at between 120 to 140 degrees C and reacts at between 175 to 195 degrees C.

42. (previously presented) The apparatus of claim 34, wherein the underfill adhesive has an elastic modulous in the range of 1 to 10 GPa.

43. (previously presented) The apparatus of claim 34, further comprising a dam around the periphery of the wafer to prevent the underfill material deposited onto the active surface of the wafer from flowing off the wafer before the partial curing of the adhesive layer.